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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/772,520	02/04/2004	Chia-Shun Hsiao	M-15212 US	5414

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EXAMINER	
CHACKO DAVIS, DABORAH	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,520	HSIAO ET AL.	
	Examiner	Art Unit	
	Daborah Chacko-Davis	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-50, are rejected under 35 U.S.C. 102(e) as being anticipated by U. S. Patent No. 6,787,415 (Chung et al., hereinafter after Chung).

Chung, in the abstract, in col 2, lines 28-67, in col 6,lines 31-67, discloses the manufacturing of a integrated circuit, wherein the integrated circuit has nonvolatile memory cells, forming a plurality of first structures (more than one) on a semiconductor substrate that projects upward, the first structure includes floating gates for a plurality of nonvolatile memory cells associated with the first structure, the first structure includes a first dielectric sidewall; forming on the semiconductor substrate pedestals (more than one) that projects upwards, the pedestal is positioned between two first structures and adjacent the first sidewalls (see reference 340 of figure 3B); forming a layer (first layer) and etching (first etch) the layer (processing the first layer) to provide a plurality of conductive lines (more than one), wherein the conductive lines overlay the first dielectric sidewall of the at least one first structure, and provide conductive gates to the memory

cells associated with the first structure, said conductive lines has a first portion that stretches between the dielectric sidewall, and the adjacent pedestal and reaches the pedestal, the second portion of the conductive line that is not located between the dielectric sidewall and the pedestal is a sidewall spacer, wherein the sidewall spacer (second portions) are not protected by a mask during the first etch (etching operation); the at least one pedestal (reference 340 of figures 3B, 5, and 6) contacts two of the conductive lines, and the two conductive lines are insulated from each other. Chung, in col 4, lines 47-67, in col 5, lines 1-25, and in col 6, lines 42-47, discloses that the first layer (material layer, conductive layer) is formed around the pedestal (a portion P1), wherein the portion (P1) extends between the tow future positions of the two conductive lines ((see figures 5, and 6), and in physical contact with the pedestal, and processing (etching) the first layer further via a second etch (to remove the portion P1, after a first etch) so as to insulate the two conductive lines from each other (claims 1-4, 22-23, and 42). Chung, in col 4, lines 56-67, in col 5, lines 1-25, discloses that the second etch is a masked etch with the portion of the first layer subjected to an anisotropic second etch, wherein the second etch is performed via a photolithographic mask, said mask can be formed over the peripheral areas of the memory cells (define gates of a peripheral transistor of the IC) (claims 5, 9, 24-25, and 29). Chung, in col 5, lines 35-36, discloses that the peripheral transistor can be formed from a layer different from the first layer (claims 6, and 26). Chung, in col 3, lines 1-55, and in figures 5-8, discloses a first structure that includes a first and second dielectric sidewall, and the first layer initially forms portions over the second dielectric sidewall, performing a third etch (isotropic third

etch performed after the anisotropic second etch) over the second sidewalls and not the first sidewall, so as to expose the first layer portions (P1) to the third etch (claims 7-8, 10, 27-28, and 30). Chung, in col 5, lines 1-17, and in figures 3B, and 5-6, discloses a first structure with a first and second sidewall, and the first layer is formed conformally over the ends (includes between the sidewalls) and around the ends of the first and second sidewalls, performing a second anisotropic etch, wherein the first etch involves etching the first layer formed on the second sidewall and not the first sidewall, and simultaneously etching the first layer portion (P1) (claims 11-12, 31-32). Chung, in col 4, lines 6-14, discloses that the pedestal comprises a conductive feature (conductive layer) that are dummy elements and not circuit elements of the IC, and that the pedestals are dummy structures with no electrical functionality (claims 13-14, 33-34, and 43-44,). Chung, in col 3, lines 10-57, discloses that dielectrics (dielectric layer) overlies the word lines (conductive lines), and that a contact opening is formed in the dielectric layer so as to expose a first portion of the conductive lines (forming a path over the word line) and allowing the formation of an electrical contact between the wordlines and a metal contact (patterned) by depositing a conductive plug in the openings, wherein the word lines (conductive lines) extend along a row of the memory cells (claims 15-17, 35-37, and 45-47). Chung, in col 3, lines 5-18, discloses that each first structure (row structure) comprises a conductive control gate line that provide control gates for the corresponding row of the memory cells (associated memory cells) (claims 18, 38, and 48). Chung, in col 6, lines 62-64, discloses that the minimum thickness of the first portion is greater than the minimum thickness of the second

portions i.e., second portions are narrower than the first portions (claims 19-20, 39-40, and 49-50). Chung, in col 6, lines 55-56, discloses that the first portions are not protected by a mask during the first etch (etching operation) (claims 21, and 41).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daborah Chacko-Davis whose telephone number is (571) 272-1380. The examiner can normally be reached on M-F 9:30 - 6:00. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark F Huff can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dcd

April 26, 2006.

JOHN A. MCPHERSON
PRIMARY EXAMINER